SYNOPSYS®

DATASHEET

RTL Architect

RTL Architect's "shift-left" strategy significantly reduces time-to-feedback

Overview

The RTL Architect™ solution is the industry's first physically aware RTL design system that significantly reduces the development cycle and delivers superior quality-of-results. RTL Architect continues the "shift-left" strategy introduced in the Synopsys Fusion Design Platform™ to address power, performance, and area (PPA) challenges earlier in the design cycle. The complexities of advanced process nodes have made it more difficult to meet PPA targets through physical implementation techniques alone, so RTL designers are tasked with exploring domain-specific architectures to dramatically improve PPA. RTL Architect provides a logical/physical workbench that can accurately predict the PPA impact of architectural changes ***without*** waiting for feedback from the physical design team.

Key Benefits

- Unified data model that provides multi-billion gate capacity and comprehensive hierarchical design capabilities
- Fast, multi-dimensional implementation prediction engine that enables RTL designers to predict power, performance, area, congestion
- Dedicated workflow environment for ease-of-use and seamless analysis of key quality metrics
- RTL re-structuring with automatic constraint updates for architectural changes and IP re-targeting
- Hierarchical floorplan creation for block area, timing, and congestion estimation
- Leverages Synopsys' world-class implementation and golden signoff solutions to deliver results that correlate-by-construction
- RTL power estimation and optimization of energy efficient designs with the PrimePower golden signoff power analysis engine
- Comprehensive cross-probing facilitates debug from layout, schematic and reports to RTL

Predictive Modeling

RTL Architect's new Predictive Engine (PE) is derived from Synopsys' implementation environment and enables rapid multi-dimensional analysis and optimization of RTL to predict PPA of downstream implementation accurately. This Predictive Engine utilizes new correct-by-construction modeling, leveraging the proven and widely used core implementation algorithms and architectures of the Synopsys Fusion Design Platform. This ensures tight correlation to the best implementation.

This also allows the RTL designers to experiment and tune their HDL code without multiple, back-and-forth, hand-offs to synthesis and to pinpoint timing bottlenecks in their source code to improve RTL quality.

Design Planning

RTL Architect's hierarchical, design planning, infrastructure automatically generates a physical implementation, with clock trees, to provide the RTL designer with accurate power, timing and area estimates. Additionally, the RTL block integrator can use the design planning capabilities to integrate in-house and third-party IP (as seen in Figure 1 Arteris® IP FlexNoC® Interconnect Integration) including bus and pipeline register planning. This fast and deep look-ahead allows the designers to not only predict but also drive physical implementation.

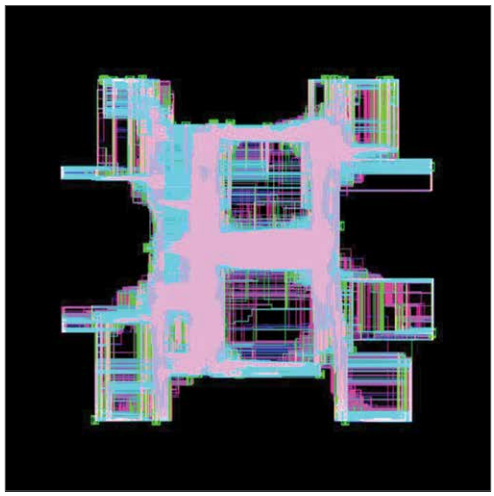


Figure 1: Arteris IP FlexNoC Interconnect Integration

RTL Design Experience

The RTL Architect experience is built around the RTL designer. The PE maps leaf cells back to the RTL so that the designer can see the direct impact a code change has on PPA. Figure 2 RTL Cross-Probing, shows the cross-probing capability from various design views to RTL. Color coded reports indicate severity level.

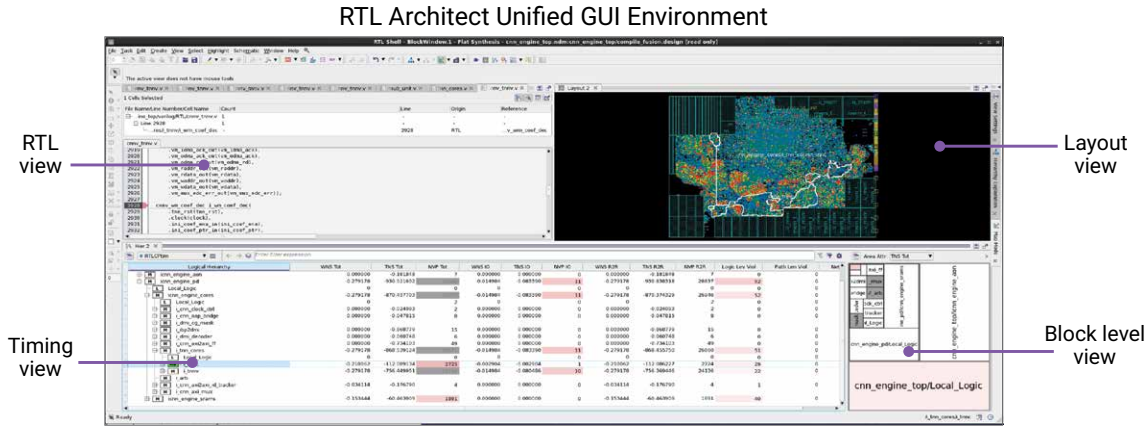
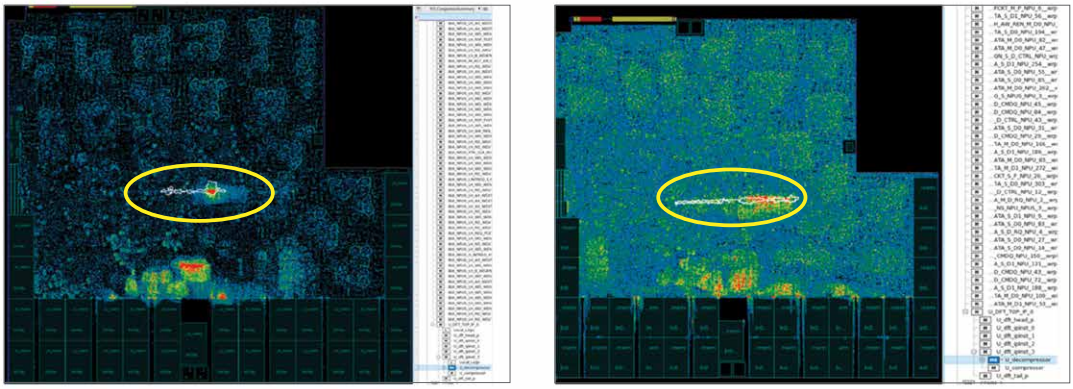


Figure 2: RTL Cross-Probing

For example, the designer can see how the logic is physically implemented by cross-probing from a report directly to the layout. This is useful for seeing the predicted congestion hotspots caused by RTL, so they can experiment with different architectures to reduce the congestion. Figure 3 shows the high degree of correlation between the place and route engines of RTL Architect and Fusion Compiler™.



RTL Architect Fusion Compiler

Figure 3: RTL Architect vs. Fusion Compiler Congestion

Another key concern for RTL designers is power usage. The interactive power summary report provides an overview of key power metrics, such as, switching and glitch power, leakage, and clock gating efficiency. The results are based on the PrimePower golden signoff power analysis engine. The report data can be sorted, filtered and cross-probed to RTL.

Bridging the Gap

RTL Architect significantly improves the quality of RTL before handing off to implementation. It addresses the limitations of the existing solutions which are hampered by inaccuracies that impact productivity as downstream implementation tools compensate. The shift-left strategy identifies and corrects physical implementation issues early in the design cycle to achieve aggressive PPA targets at advanced nodes through better RTL.